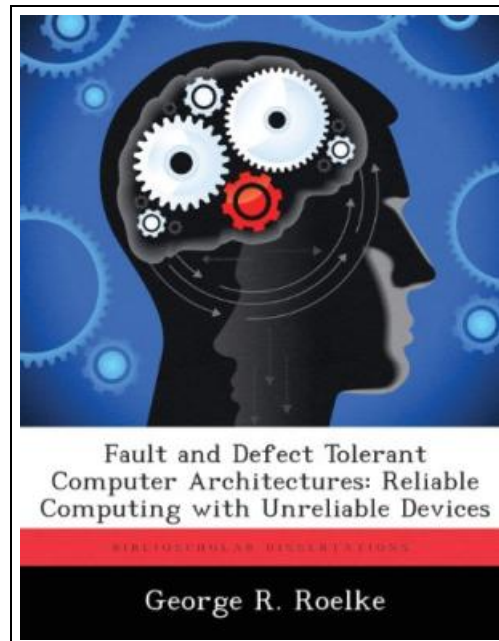# Fault and Defect Tolerant Computer Architectures: Reliable Computing with Unreliable Devices (Paperback)

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Reviews

This is the finest publication we have read through right up until now. Better then never, though i am quite late in start reading this one. Its been written in an remarkably easy way in fact it is only after i finished reading through this book by which basically altered me, affect the way i think.

(Dr. Gabriella Hayes)

FAULT AND DEFECT TOLERANT COMPUTER ARCHITECTURES: RELIABLE COMPUTING WITH UNRELIABLE DEVICES (PAPERBACK)

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Biblioscholar, United States, 2012. Paperback. Condition: New. Language: English . Brand New Book ***** Print on Demand *****.As conventional silicon Complementary Metal-Oxide-Semiconductor (CMOS) technology continues to shrink, logic circuits are increasingly subject to errors in- duced by electrical noise and cosmic radiation. In addition, the smaller devices are more likely to degrade and fail in operation. In the long term, new device technolo- gies such as quantum cellular automata and molecular crossbars may replace silicon CMOS, but they have significant reliability problems. Rather than requiring the cir- cuit to be defect-free, fault tolerance techniques incorporated into an architecture allow continued system operation in the presence of faulty components. This research addresses construction of a reliable computer from unreliable de- vice technologies. A system architecture is developed for a fault and defect tolerant (FDT) computer. Trade-offs between different techniques are studied, and the yield of the system is modelled. Yield and hardware cost models are developed for the fault tolerance techniques used in the architecture. Fault and defect tolerant designs are created for the processor, and its most critical component, the cache memory.

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