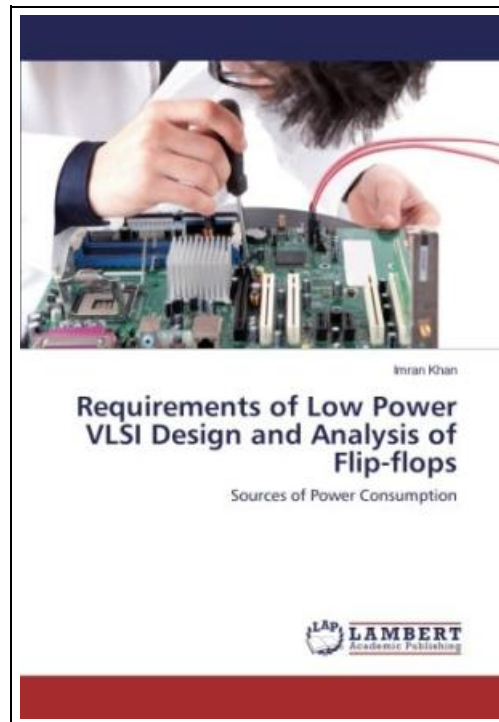# Requirements of Low Power VLSI Design and Analysis of Flip-flops

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Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Sources of Power Consumption | In recent years, power consumption has become a critical design concern due to the growing demand of portable applications and the increasing costs incurred and difficulties encountered in cooling and heat removal processes. Flip-flops are heavily studied circuits, as they have a large impact on both cycle time and power consumption in modern synchronous systems. In many digital VLSI designs, the clock system that includes clock distribution network and flip-flops is one of the highest power consuming component. Therefore, flip-flops should be designed to consume minimum power, while not compromising on area, delay and reliability. This book begins with the basic background information about power consumption and significance of low power design. Different types of power consumption are also discussed. Different state-of-the-art master slave Single edge triggered flip-flops (SETFFs) are reviewed and implemented on TSPICE using BSIM models. The nominal simulation conditions, along with analysis and optimization performed during simulation, are discussed. In this book, simulation results of flip-flops are compared. | Format: Paperback | Language/Sprache: english | 76 pp.

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