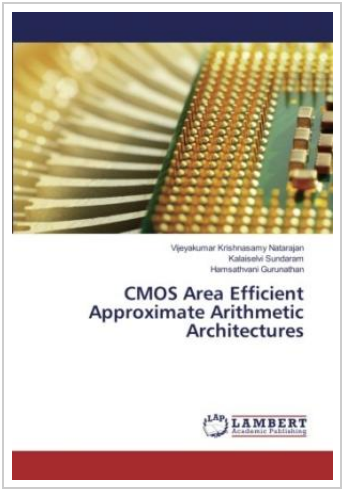

CMOS Area Efficient Approximate Arithmetic Architectures

By Krishnasamy Natarajan, Vijeyakumar / Sundaram, Kalaiselvi

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Approximate computation provide alternate solution to reduce energy consumption of high performance present day DSP application devices. Conventional multiplication and addition techniques consume a lot of energy. In this brief design of approximate arithmetic units for signal processing application is explored. First an approximate adder is proposed by changing the logic of basic full adder cell. The proposed adder cell has fewer transistor count compared to recent similar approach. Next, an approximate multiplier with low error is designed using lead one detection and selecting n/2 bits for an n bit input. The proposed n/2 bit approximate multiplier performs well in terms of error and power performance compared to recent similar approach. In continuation the approximate units are implemented in a Multiply-Accumulate(MAC) unit. The proposed approximate MAC unit provides significant improvement in power, area, and delay at the cost of little degrade in accuracy. Finally, the proposed MAC unit is implemented in filtering application to verify the functionality. | Format: Paperback | Language/Sprache: english | 60 pp.

Reviews

This type of publication is almost everything and helped me looking forward and much more. I am quite late in start reading this one, but better then never. You wont really feel monotony at whenever you want of your own time (that's what catalogs are for relating to if you ask me).

-- ***Prof. Buddy Leuschke***

This book is very gripping and fascinating. Yes, it is play, nonetheless an interesting and amazing literature. I found out this ebook from my dad and i recommended this pdf to discover.

-- ***Lavada Nikolaus***